UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,925	07/24/2000	Yong jin Park	9898-156	4905

7590 02/12/2003

Marger Johnson & McCollom Pc
1030 SW Morrison Street
Portland, OR 97205

EXAMINER
NGUYEN, MIKE

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/621,925	PARK ET AL.	
	Examin r	Art Unit	
	Mike Nguyen	2182	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-16* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-16 are pending for the examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3 and 5-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiroyuke Noji (U.S. Pat. No. 6,138,255).

4. As to claim 3, Noji teaches a semiconductor memory device, comprising:

a first plurality of pads adapted to receive a corresponding plurality of first external signals (see figure 2 elements 10, 10S and column 4 lines 15-22);

a second plurality of pads adapted to receive a corresponding plurality of second external signals (see figure 2 element 20 "ADR[0] to ADR[n]" and column 4 lines 15-22); and

an input and output mode set circuit coupled to the first and second plurality of pads and

adapted to generate a plurality of input and output mode signals responsive to the plurality of first and second external signals (see figure 2 elements 50, 60, 70 and column 4 lines 59-67 and column 15 lines 1-10);

wherein, during a test mode, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive only to the plurality of first external signals, the plurality of the first pads receiving a high voltage higher than a voltage level of a power supply signal thereby generating a plurality of first external signals having a level higher than a voltage level of the power supply signal (see figure 2 elements 60, 70, 40NS and column 4 lines 25-29, 66-67 and column 5 lines 3-10 wherein the level detecting 60 detects whether the reference signal 10S has low, high, or same as external signal. If voltage level of reference signal 10S is set at lower than the voltage level of external signal, it is in test mode and the selecting circuit 70 selects only the signal 40NS responsive to the first external signals);

wherein, during normal operations, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to the plurality of second external signals, the plurality of second external signals having logic levels (see column 4 lines 43-48).

5. As to claim 5, Noji teaches the semiconductor memory device of claim 3 wherein the power supply signal is applied to the semiconductor memory device after the high voltage is applied to one of the first plurality of pads (see figure 3 and column 5 lines 15-27).

6. As to claim 6, Noji teaches the semiconductor memory device of claim 10 wherein the plurality of second pads float (see figure 2 element "ADR[0] to ADR[n]" wherein the plurality of pads is not connect each other).

7. As to claim 7, Noji teaches the semiconductor memory device of claim 3 wherein at least one of the plurality of second pads is grounded to a ground terminal of the semiconductor memory device (see figure 4A).

8. As to claim 8, Noji teaches the semiconductor memory device of claim 3 wherein the input and output mode set circuit comprises:

a pad circuit coupled to the first plurality of pads and adapted to generate a plurality of first signals, one of the plurality of first signals being active when the high voltage is applied to at least one of the plurality of pads (see figure 2 elements 10, 10S and column 4 lines 15-22);

a control signal generating circuit adapted to generate a plurality of control signal responsive to the plurality of first signals and a plurality of second signals (see figure 2 elements 50, 60); and

an input and output mode signal generating circuit adapted to generate the plurality of input and output mode signals responsive to the plurality of control signals and the plurality of second external signals (see figure 2 element 70 and column 5 lines 3-10).

9. As to claim 9, Noji teaches the semiconductor memory device of claim 8 wherein the plurality of second signals comprises a power supply sense signal activated when the power supply signal has a level equal to or greater than a predetermined level and input and output mode control signal activate responsive to a write enable signal, a row address strobe signal, and a column address strobe signal (see figure 2 element 60 and column 4 lines 66-67 and column 5 lines 1-2).

10. Claims 1, and 2 are of similar scope as claims 3-9 are therefore rejected under same rationale.

11. Claims 10, and 12-15 are of similar scope as claim 3-9 and are therefore rejected under same rationale.

12. As to claim 11, Noji teaches the semiconductor memory device of claim 10 wherein each of the plurality of pads float (see figure 2 element 10S, "ADR[0] to ADR[n]" wherein each of the plurality of pads is not connect each other).

13. As to claim 16, Noji teaches the semiconductor memory device of claim 10 wherein the plurality of pads includes two pads (see figure 2 element 10S, "ADR[0] to ADR[n]").

Allowable Subject Matter

14. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Mike Nguyen
Patent Examiner
Group Art Unit 2182

01/24/2003

Recent Statutory Changes to 35 U.S.C. § 102(e)

On November 2, 2002, President Bush signed the 21st Century Department of Justice Appropriations Authorization Act (H.R. 2215) (Pub. L. 107-273, 116 Stat. 1758 (2002)), which further amended 35 U.S.C. § 102(e), as revised by the American Inventors Protection Act of 1999 (AIPA) (Pub. L. 106-113, 113 Stat. 1501 (1999)). The revised provisions in 35 U.S.C. § 102(e) are completely retroactive and effective immediately for all applications being examined or patents being reexamined. Until all of the Office's automated systems are updated to reflect the revised statute, citation to the revised statute in Office actions is provided by this attachment. This attachment also substitutes for any citation of the text of 35 U.S.C. § 102(e), if made, in the attached Office action.

The following is a quotation of the appropriate paragraph of 35 U.S.C. § 102 in view of the AIPA and H.R. 2215 that forms the basis for the rejections under this section made in the attached Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying references, except when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. For such patents, the prior art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

The following is a quotation of the appropriate paragraph of 35 U.S.C. § 102 prior to the amendment by the AIPA that forms the basis for the rejections under this section made in the attached Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

For more information on revised 35 U.S.C. § 102(e) visit the USPTO website at www.uspto.gov or call the Office of Patent Legal Administration at (703) 305-1622.